

GP Kangra

TRAINING PROCESS ADEQUACY
FACULTY REPORT

1 Department Electronics & Communication Engineering
 Teacher's Name Jagdeep Singh
 Course Diploma in E.C.E Duration 03 years From 2024 To 2026
 Subject Digital Electronics Total no of period 56

2 Report:

- Delivery needs: - Adequate/ Less then adequate (give details)

- Improvements recommended- Adequate

Date 01/8/2025

[Signature]
Faculty/ Instructor

3 Comments and recommendation:

Date 01/8/2025

[Signature]
HOD

4 Decision /directions:

Date-----

[Signature]
Principal

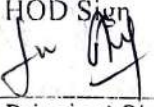
PLANNED SYLLABUS COVERAGE(Theory)

G P Kangra		Department: <u>E-C-E</u> Subject <u>Digital electronics</u>				
SYLLABUS COVERAGE		Course <u>Diploma in E-C-E</u> Duration <u>03 years.</u>				
		Total Periods <u>56</u> Theory <u>56</u>				
Sr. No.	Period Nos.	Topic	Details	Instruction Reference	Additional Study Recommended	Remarks
1.	1 to 12.	Number system & Boolean Algebra.	Introduction to different no systems - Binary octal decimal Hexadecimal. Conversion from one number system to another. Boolean variables - Rules & Laws of Boolean algebra. De-morgan theorem - K-maps & their use for simplification of Boolean expression.			
2.	13 to 26	Logic Gates	AND, OR, NOT, NAND, NOR, XOR & NOR: Symbolic representation & truth Table: Implementation of Boolean expressions & Logic functions using gates Simplification of expression.			
3.	27 to 38	Combinational Logic Circuits	Arithmetic ckt's - Addition, subtraction, 2's & 2's complement. Half Adder, Full Adder, Half sub. & Full sub. Parallel & series adders. Encoder, Decoder Multiplexer 2:1, 4:1, 8:1 mux & their Applications, Demultiplexer 1:2 1:4 & 1:8 Demux.			
4.	39 to 47	Sequential Logic Ckts	Flip Flops - SR, JK, T, D, JKMS., Triggering. Counters: 46A. UP-down counter, for Asynchronous ripple counter, Decade counter mod 3 mod 7 counter - Johnson Counter, Ring Counter. Register			

Sr. No.	Period Nos.	Topic	Details	Instruction Reference	Additional Study Recommended	Remarks
5.	48 to 56	Memory Devices	- 4 bit shift register, SISO, SIPO, PISO & PIPO. Classification of Memories. RAM organization, Address lines & Memory Size, static RAM, Bipolar RAM, Cell dynamic RAM, DRAM, DDR RAM. Read only Memory - ROM organization, Expanding memory, PROM, EPROM, EEPROM, Flash memory. Data Converters. Digital to analog Converters. Analog to Digital converter.			

Extra Topics to be covered beyond the scope of the syllabus (as required by industry/ as recommended by Teacher which he/ she finds necessary)

Sr. No.	Period No.	Topic Covered	Instruction Reference	Additional Study recommended	Remarks

Approved / Not approved	
Date 01/01/2025	HOD Sign 
Date	Principal Sign 

Department: *Electronics Comm. Engg*
 Course: *Diploma in E.C.E*

Practical Planning & Coverage Status

Laboratory: *Digital Electronics Lab/Allen*
 Subject: *Digital Electronics*

Sr. No.	Details of Practical	Availability of		Likely Turn/Date	Actual Date	Responsibility	HOD Sign.	Remarks
		Equipment Set up	STD Ref. Write up					
1.	To verify the truth tables for all logic gates using AND, OR, XOR, X-NOT using C-mos logic gates & TTL logic gates	Standard Trainer 141	Trainer's Manual,					
2.	Implementation & realization of combinational logic gates using IC's.							
3.	Implementation of A.A, F.A, 4-bit FLS							
4.	Implementation of parallel & serial F.A using IC's.							
5.	Design & development of multi/mux & De-mux using multi/mux IC's.							
6.	Verification of the function of SR, D, JK & T F.F.							
7.	Design controlled shift register							
8.	Construction of single digit decade counter (0-9) with 7 segment display.							
9.	Design of a program able display.							

Department:
Course:

Subject:

Sr. No.	Details of Practical	Availability of		Likely Turn/Date	Actual Date	Responsibilit	HOD Sign.	Remarks
		Equipment Set up	STD Ref. Write up					
	- segment display.							
10.	Study of different memory I.C's.							
11.	Study Digital to analog and analog to digital converter.							
12.	Simulate in Software (Circuit Spice) an analog to digital converter.							

05

GP Kangra

TRAINING PROCESS ADEQUACY
FACULTY REPORT

- 1 Department Electronics & Communication Engineering
Teacher's Name Tagdeep Singh
Course Diploma in E.C.E. Duration 03 years From 2024 To 2026
Subject F.I.E.M. Total no of period 56

2 Report:

- Delivery needs: - Adequate/ Less then adequate (give details)
- Improvements recommended- Adequate

Date 01/08/2025
Faculty/ Instructor

3 Comments and recommendation:

Date 01/05/2025
HOD

4 Decision /directions:

Date-----


Principal

PLANNED SYLLABUS COVERAGE(Theory)

GPK-F-17

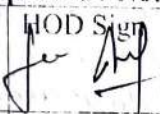
G P Kangra		Department: <u>E.C.E.</u> Subject <u>E.T. P.M.</u>				
SYLLABUS COVERAGE		Course <u>Diploma in E.C.E.</u> Duration <u>03 years</u>				
		Total Periods <u>56</u> Theory <u>56</u>				
Sr. No.	Period Nos.	Topic	Details	Instruction Reference	Additional Study Recommended	Remarks
1.	1 to 04	Basic of Measurement.	- Measurement, method of measurement, types of instruments. - Specifications of Inst: Accuracy, Precision, Sensitivity, Resolution, Range, errors in measurement, source of errors, Loading effect, imp & applications of standards & calibration			
2.	5 to 18	Transducers	- Distinction b/w active & passive transducers with exam: Basic requirement of transducers. - Principles of operation of the following transducers & their applications in measuring the physical quantity - variable Resistance type - - variable capacitance type - other, C.R. & D.C. sensor etc. - construction & working of CRT - Block diagram of CRO - Specification of CRO & explanation - Measurement of current, voltage, freq, time period & Phase using CRO - Digital storage oscilloscope (DSO)			
3.	19 to 30	Cathode Ray oscilloscope	- Principles of measurement of DC voltage, DC current, AC voltage, AC current. - Principles of operation & construction of (PMMC) & moving Iron type Instruments			
4.	31 to 38	Voltage (current) & Resistance measurement.	- Explanation of Block diagram - Specifications of low frequency & RF generator, Pulse generator			
5.	39 to 47	Signal Generators & Analytical Instruments.				

To be approved from concerned HOD within seven days from beginning of semester & will be kept with the concerned teacher in his file.

Sr. No.	Period Nos.	Topic	Details	Instruction Reference	Additional Study Recommended	Remarks
6.	48 to 57	Digital Instruments.	- function generators - Distortion factor meter - Induction Amplifiers characteristics, need & working - Comparison of Analog & Digital Instruments - Working Principle of semi. dual slope & integration type digital voltmeter - Block diagram & working of digital multimeter - Specification of digital multimeter & their application - Limitations of digital multimeters.			

Extra Topics to be covered beyond the scope of the syllabus (as required by industry/ as recommended by Teacher which he/ she finds necessary)

Sr. No.	Period No.	Topic Covered	Instruction Reference	Additional Study recommended	Remarks

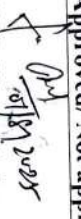
Approved / Not approved	
Date 01/08/2025	HOD Sign 
Date	Principal Sign 

C P Kangra Practical Planning & Coverage Status

Department:
Course:

Laboratory:
Subject:

Sr. No.	Details of Practical	Availability of		Likely Turn/Date	Actual Date	Responsibility	HOD Sign.	Remarks
		Equipment Set up	STD Ref. Write up					
1.	To observe the loading effect of a multimeter while measuring voltage across load, resistance & high resistance.	Standard Trainer kit.	Trainer kit. manual					
2.	To observe the limitation of multimeter for measuring high frequency voltage							
3.	Measurement & plot of characteristics of optical device like photo diodes & photo cells							
4.	Characteristics of light operated switch using photo-transistor & LDR							
5.	Measurement of strain using strain gauge & thermocouple.							
6.	Measurement of temperature using thermistor & thermocouple							
7.	Measurement of linear & angular displacement							

Approved/ Not approved

 HOD Sign with date

Principal Signature with date


Department:

Course:

Laboratory:

Subject:

Approved/ Not approved

Approved/ Not approved

HOD Sign with date

Principal Signature with date

Dr. F.

PLANNED SYLLABUS COVERAGE (Theory)

GPKE-F-17

Department: <u>EEE</u> Subject <u>ECN</u>	
Course <u>Diploma</u>	Duration <u>3 years</u>
Total Periods <u>T-58</u>	
Topic	Details
Basics of Network & Network Theorem	Node & Mesh Analysis Superposition theorem Thevenin theorem Norton Theorem Max. Power Transfer Theorem Reciprocity Theorem
Graph Theory	Concept of Graph Node tree of Network and incidence matrix Analysis of resistive network using cut set and tie-set. Duality theorem and their application in the electrical ckt.
Time Domain & Frequency domain analysis	Solution of I & II order differential equations for series & parallel R-L, R-C R-L-C ckt. Initial & final conditions in network elements. Forced & free response Time constant, Steady state & Transient state response. Analysis of electrical ckt using Laplace transform for std inputs (unit, Ramp, step)

The approved from concerned HOD within seven days from beginning of semester & will be kept with the concerned teacher as file.

Sr. No.	Period Nos.	Topic	Details	Instruction Reference	Additional Study Recommended
4			Discrete spectra & exponential response of linear systems steady state response of network to a sinusoidal periodic input. Transfer function, effective power factor, effective values. Fourier transform & continuous spectra. Introduction to the two port N/m and various N/m parameters. S.C. " " " " Transmission parameters Hybrid parameters	- do -	- do -
5		Two Port Network			

Extra Topics to be covered beyond the scope of the syllabus (as required by ind recommended by Teacher which he/she finds necessary)

Sr. No.	Period No.	Topic Covered	Instruction Reference	Additional Study Recommended

Approved / Not approved	
Date 01/8/2025	HOD Sign 
Date 01/08/2025	Principal Sign 

Use additional sheets (if required).

Sr. No.	Details of Practical	Availability of		Likely Turn/Date	Actual Date
		Equipment	STD Ref. Write up		
1.	Construct the CRT & plot the VI char. of PN diode & find cut in voltage.	PN diode kit			
2.	Construct the CRT and plot the VI char. of Zener diode. Find the breakdown voltage.	Zener diode kit			
3.	Construct a Half wave rectifier and obtain regulation charact. with out filter & with filter and compare the result.	Half wave Rectifier kit			
4.	Construct a full wave center tap rectifier and obtain regulation charact. without filter & with filter and compare the result.	Full wave Rectifier kit			
5.	Construct a bridge rectifier and obtain regulation charact. without filter & with filter.	Full wave Rectifier kit			

C P Kangra Practical Planning & Coverage Status

Department:
Course:

Laboratory:
Subject:

Sr. No.	Details of Practical	Availability of			Likely	Actual Date	Responsibility	HOD Sign.
		Equipment	STD Ref.	Write up				

6. Obtain the character. of Diac & Triac.
7. Simulate Half wave, Full wave and bridge rectifier using simulation software.
8. PSPICE
9. Diac/ Triac
10. Turn on / off
11. Write up
12. Simulation
13. PSPICE
14. Software
15. Rectifier using simulation software
16. Full wave bridge rectifier using simulation software
17. Full wave bridge rectifier using simulation software
18. Full wave bridge rectifier using simulation software
19. Full wave bridge rectifier using simulation software
20. Full wave bridge rectifier using simulation software
21. Full wave bridge rectifier using simulation software
22. Full wave bridge rectifier using simulation software
23. Full wave bridge rectifier using simulation software
24. Full wave bridge rectifier using simulation software
25. Full wave bridge rectifier using simulation software
26. Full wave bridge rectifier using simulation software
27. Full wave bridge rectifier using simulation software
28. Full wave bridge rectifier using simulation software
29. Full wave bridge rectifier using simulation software
30. Full wave bridge rectifier using simulation software
31. Full wave bridge rectifier using simulation software
32. Full wave bridge rectifier using simulation software
33. Full wave bridge rectifier using simulation software
34. Full wave bridge rectifier using simulation software
35. Full wave bridge rectifier using simulation software
36. Full wave bridge rectifier using simulation software
37. Full wave bridge rectifier using simulation software
38. Full wave bridge rectifier using simulation software
39. Full wave bridge rectifier using simulation software
40. Full wave bridge rectifier using simulation software
41. Full wave bridge rectifier using simulation software
42. Full wave bridge rectifier using simulation software
43. Full wave bridge rectifier using simulation software
44. Full wave bridge rectifier using simulation software
45. Full wave bridge rectifier using simulation software
46. Full wave bridge rectifier using simulation software
47. Full wave bridge rectifier using simulation software
48. Full wave bridge rectifier using simulation software
49. Full wave bridge rectifier using simulation software
50. Full wave bridge rectifier using simulation software
51. Full wave bridge rectifier using simulation software
52. Full wave bridge rectifier using simulation software
53. Full wave bridge rectifier using simulation software
54. Full wave bridge rectifier using simulation software
55. Full wave bridge rectifier using simulation software
56. Full wave bridge rectifier using simulation software
57. Full wave bridge rectifier using simulation software
58. Full wave bridge rectifier using simulation software
59. Full wave bridge rectifier using simulation software
60. Full wave bridge rectifier using simulation software
61. Full wave bridge rectifier using simulation software
62. Full wave bridge rectifier using simulation software
63. Full wave bridge rectifier using simulation software
64. Full wave bridge rectifier using simulation software
65. Full wave bridge rectifier using simulation software
66. Full wave bridge rectifier using simulation software
67. Full wave bridge rectifier using simulation software
68. Full wave bridge rectifier using simulation software
69. Full wave bridge rectifier using simulation software
70. Full wave bridge rectifier using simulation software
71. Full wave bridge rectifier using simulation software
72. Full wave bridge rectifier using simulation software
73. Full wave bridge rectifier using simulation software
74. Full wave bridge rectifier using simulation software
75. Full wave bridge rectifier using simulation software
76. Full wave bridge rectifier using simulation software
77. Full wave bridge rectifier using simulation software
78. Full wave bridge rectifier using simulation software
79. Full wave bridge rectifier using simulation software
80. Full wave bridge rectifier using simulation software
81. Full wave bridge rectifier using simulation software
82. Full wave bridge rectifier using simulation software
83. Full wave bridge rectifier using simulation software
84. Full wave bridge rectifier using simulation software
85. Full wave bridge rectifier using simulation software
86. Full wave bridge rectifier using simulation software
87. Full wave bridge rectifier using simulation software
88. Full wave bridge rectifier using simulation software
89. Full wave bridge rectifier using simulation software
90. Full wave bridge rectifier using simulation software
91. Full wave bridge rectifier using simulation software
92. Full wave bridge rectifier using simulation software
93. Full wave bridge rectifier using simulation software
94. Full wave bridge rectifier using simulation software
95. Full wave bridge rectifier using simulation software
96. Full wave bridge rectifier using simulation software
97. Full wave bridge rectifier using simulation software
98. Full wave bridge rectifier using simulation software
99. Full wave bridge rectifier using simulation software
100. Full wave bridge rectifier using simulation software

8. Develop a simulation model for voltage series series 2.5 shunt feedback and plot a/p. compare the result for simulation model & developed ckt. Develop a model for current series and current shunt feedback amplifier. Develop ckt for current series & current shunt feedback amp & obtain a/p. compare result for both. -do -

Approved/Not approved
HOD Sign with date
11/10/18/23